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# A low power 12-bit and 25-MS/s pipelined ADC for the ILC / Ecal integrated readout

RARBI Fatah, DZAHINI Daniel, *Member, IEEE*, Laurent GALLIN-MARTEL

**Abstract**—The design of a fully integrated electronics readout for the next ILC ECAL presents many challenges. Low power dissipation is required, and it will be necessary to integrate together the very front-end stages with an analog to digital converter. We present here two prototypes of a 12-bit 25-MS/s analog to digital converter using a pipelined architecture. The first one is composed of ten 1.5 bit stages and a 2 bit full flash ADC which produces the least significant bits (LSB) of the converter. The second prototype is composed of a multi-bit first stage of 2.5 bits, followed by seven 1.5 bit stages as a back-end converter and a 3 bit full flash. A CMOS 0.35  $\mu\text{m}$  process is used, and the dynamic range covered is 2V. The analog part of the converter can be quickly (a couple of  $\mu\text{s}$ ) switched to a standby mode that reduces the DC power dissipation by a ratio of 1/1000. The total power dissipation of the first prototype is 37mW. For the second chip, the size of the converter's layout including the digital correction stage is only 1.9mm\*0.9mm, and the total power dissipation is 42mW.

## I. INTRODUCTION

FOR the next International Linear Collider (ILC), the front-end electronics for the electromagnetic calorimeter is really challenging. Mechanical constraints lead to the necessity to integrate in the same chip many different critical stages of the read-out electronics: charge preamplifiers, multi gain shapers, analog memories, ADC, and digital back-end. The design of the analog to digital converter must deal with the power dissipation constraint which is one of the main concerns for the electronics. We present here two prototypes of a high speed converter configuration designed to multiplex many analog channels to one ADC as shown in figure 1. This design makes the assumption that a high speed converter helps to minimize the cross talk and the total power dissipation.

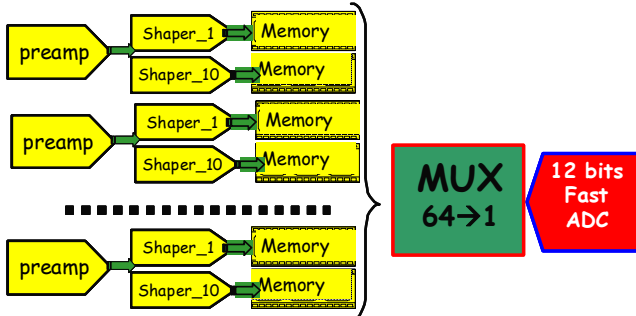


Figure 1: Overview of the front end read out in high speed configuration

A pipelined architecture is used. For high dynamic converters ( $>10$  bit), and high speed (beyond 10MHz), this architecture is usually considered as a good compromise between the power dissipation and the speed [1]-[4]. An overview block diagram is shown in figure 2.

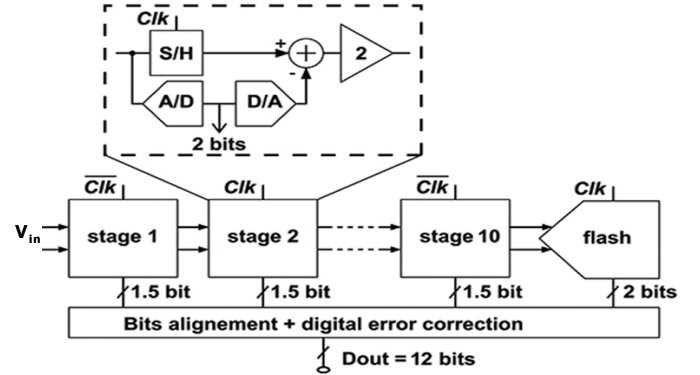


Figure 2: General block diagram of a pipelined converter

The ADC is composed of a set of pipelined stages. Each stage produces a digital estimate of an incoming held signal, then converts this estimate back to the analog, and subtracts the result from the held input. This residue is then amplified before being transferred to the next stage. Eventually the last stage is a full flash converter which determines the least significant bit (LSB). The successive digital results from the pipelined stages are appropriately delayed throughout a bit alignment network. Then a digital correction stage helps to recover the errors due to the offset of the comparators. Therefore, low offset comparators are not necessary and the total power consumption is reduced. The power dissipation is optimized for each stage following a power scaling in the successive pipeline stages.

This paper summarizes hereafter the design of two prototypes of the converter and we present some testing results. Both chips were implemented without calibration or trimming approaches [5].

## II. THE PIPELINE ADC

### A. The 1.5 bit stage

The converter consists of ten 1.5 bit sub-ADC followed by a 2 bit full flash stage (refer to figure 2).

Figure 3 illustrates a very simplified diagram of a 1.5 bit pipeline stage. The actual implementation in our design is differential. The A/D block consists of two non critical comparators. The D/A conversion, subtraction, amplification, and S/H functions are performed by a switched capacitor

This work is on behalf The CALICE Collaboration.

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$\alpha$  is set to 0 or 1 or -1, depending on the output codes (b0, b1);  $\pm V_{\text{ref}}$  specifies the dynamic range.

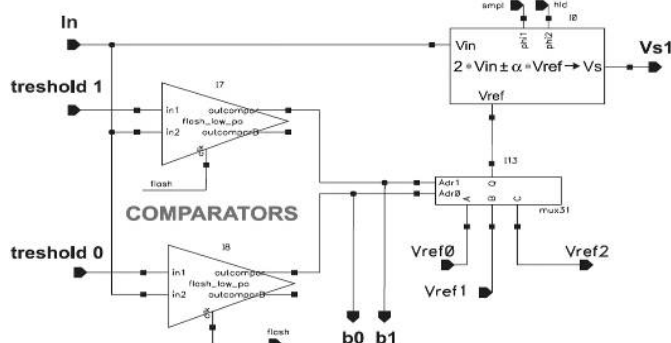


Figure 3: Bloc diagram of a 1.5 bit sub-converter stage.

In figures 4 is shown the output codes for a 2 V peak-to-peak dynamic range with a 1 MHz sine wave input signal.

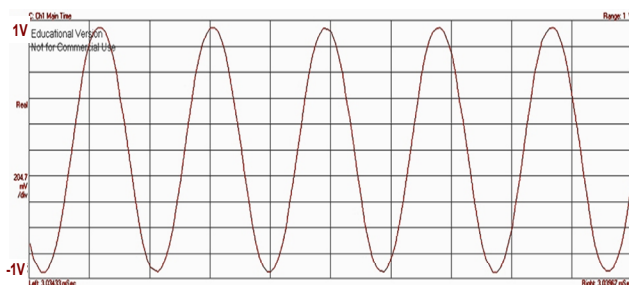


Figure 4: Output codes for an input 2V peak-to-peak sine wave

The Differential Non linearity (DNL) and the Integral Non Linearity (INL) are presented respectively in figure 5 and 6.

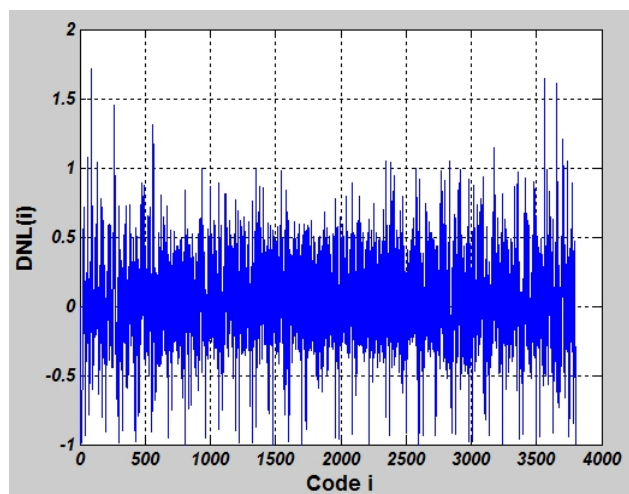


Figure 5: Linearity results (DNL)

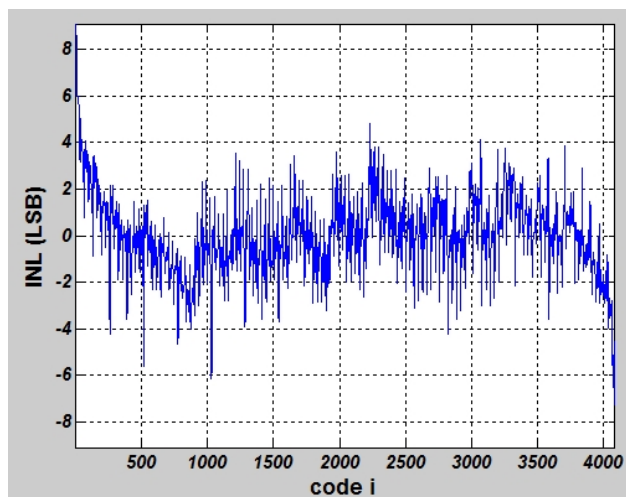


Figure 6: Linearity results (INL)

The DNL is almost  $\pm 1\text{LSB}$ , and the INL is  $\pm 4\text{LSB}$ .

This prototype deals with CALICE requirements and it is closed to the capacitors matching limits of a .35 $\mu$ m process. One solution to improve further the linearity and the total power consumption is to include a first multi-bit stage. Thus a second prototype was designed. This new version produces 2.5 bits in the first stage followed with seven 1.5 bit stages and a last 3 bits full flash. The architecture of this second prototype is illustrated in figure 7.

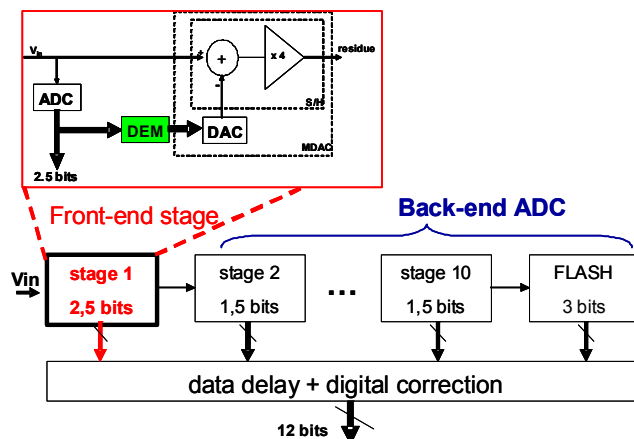


Figure 7: Block diagram of a pipelined converter with a multi-bit stage

### B. The 2.5 bit stage

In figure 7 is shown a very simplified diagram of a 2.5 bit stage as a front end stage of the pipeline converter. The ADC block consists of six non critical comparators. The DAC conversion, subtraction, amplification, and S/H functions are performed by a switched capacitor structure as one can see in figure 8. This block is the multiplier-DAC (MDAC). It is composed of four capacitors.

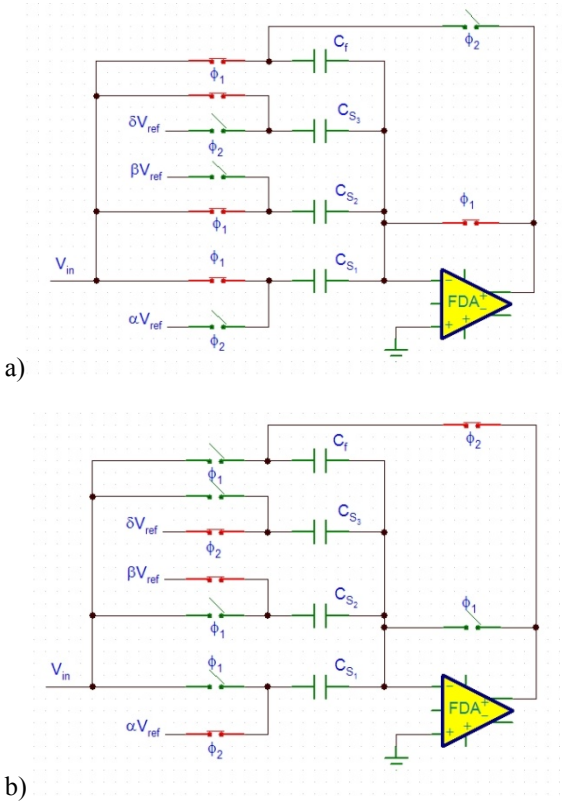


Figure 8: A 2.5 bits MDAC a) sampling phase; b) amplifying

The incoming signal is sampled during phase “ $\Phi_1$ ” (figure 8 a). It is amplified by charge redistribution during phase “ $\Phi_2$ ” (figure 8 b)). During this amplification phase, one plate of the sampling capacitors ( $C_{s_i}$ ) is connected to a reference voltage  $V_{refi}$  which will be subtracted from the amplified signal. The residue resulting from this operation is transmitted to the next pipeline stage. The value selected for  $V_{refi}$  is respectively 0 or  $(-V_{ref})$  or  $(V_{ref})$  depending on the comparators outputs. The amplification gain is 4. Hence the transfer function of this stage is:  $V_s = 4 \cdot V_{in} - (\alpha + \beta + \gamma) \cdot V_{ref}$  where  $\alpha$ ,  $\beta$  and  $\gamma$  are set to 0, -1 or 1, depending on the output codes of the sub-ADC.  $\pm V_{ref}$  specifies the dynamic range. The transfer characteristic for a 2.5 bit stage is shown in figure 9.

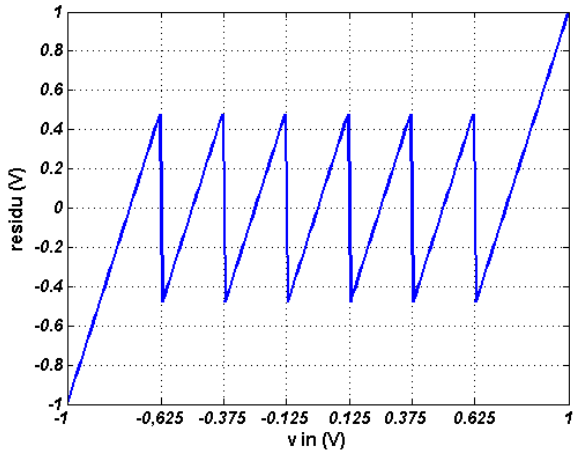


Figure 9: A 2.5 bit residue transfer curve

The expression “2.5 bit” is used to emphasize that only 7 combinations out of the 8 are acceptable for the output codes. The code (1, 1, 1) is avoided, thereby the amplifier will not saturate and this leaves room for the digital error correction.

The sub-ADC is composed of 6 low offset and low power static comparators. The simplified schematic of the comparator is shown in figure 10.

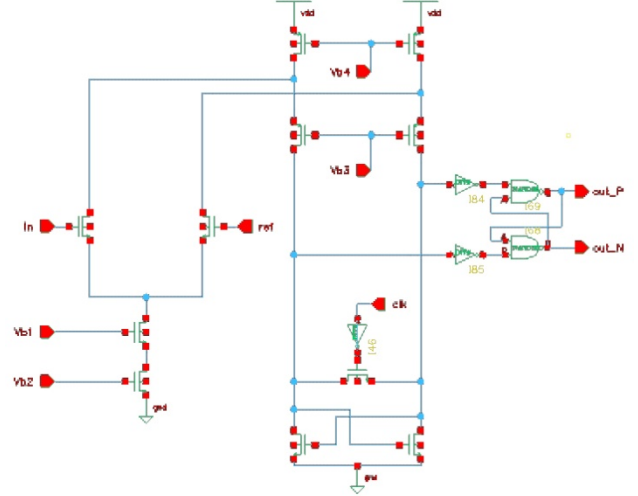


Figure 10: The static comparator

The maximum offset of these comparators must be limited to  $V_{ref}/8$ , where  $\pm V_{ref}$  is the full dynamic range. The comparator is based on a folded cascode amplifier with a positive feedback. It consumes less than 150  $\mu W$ , and its offset is less than  $\pm 40 mV$  as one can see in the Monte Carlo simulations in figure 11.

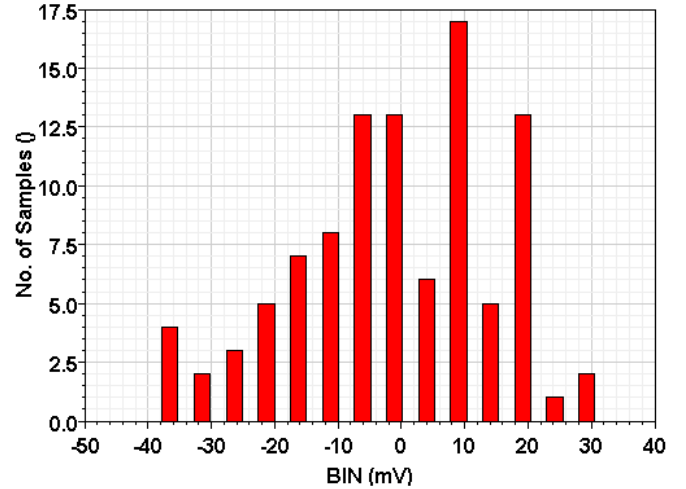


Figure 11: Offset of static comparator (monte carlo simulation with 100 bins)

The output codes from the comparators are used thereafter by the DAC to rebuild the analog residue. A precise amplification by 4 is performed by four equivalent capacitors as shown in figure 8. The matching of  $C_f$  with all  $C_s$  is the main issue for this amplification, and it is the main source of non linearity for the converter.

To expect a 12 bit resolution feature, the amplifier in the first stage must have a high open loop gain (more than 72 dB). The folded-cascode architecture used is shown in figure 12.

Auxiliary amplifiers are added to increase the open loop gain [6], at just a little expense of power dissipation. The Bode diagram simulations results are given in figure 13.

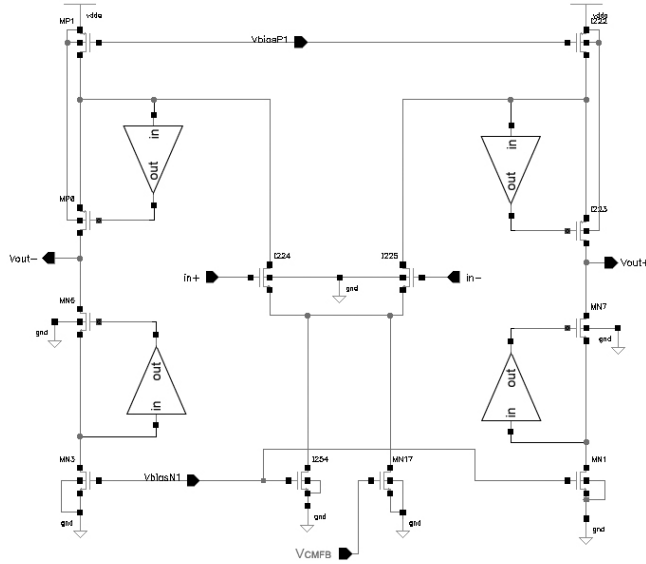


Figure 12: A regulated folded-cascode OTA

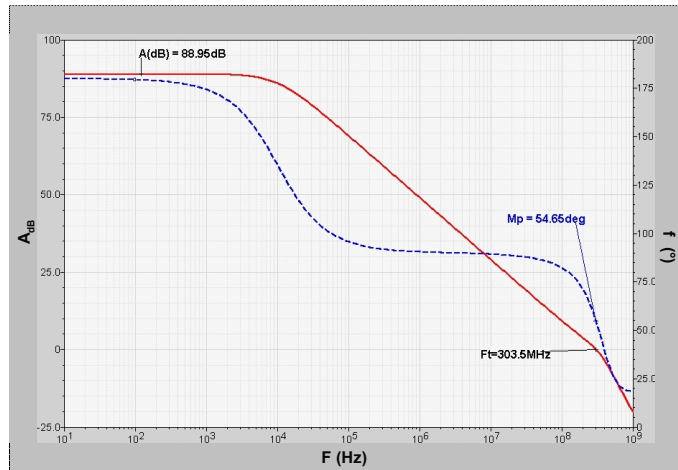


Figure 13: Bode diagram for the OTA on a 3pF load.

The linearity simulations of our first Multiplier and DAC stage are given in Figure 14. One can notice a full range integral non linearity (INL) in the order of 1 LSB.

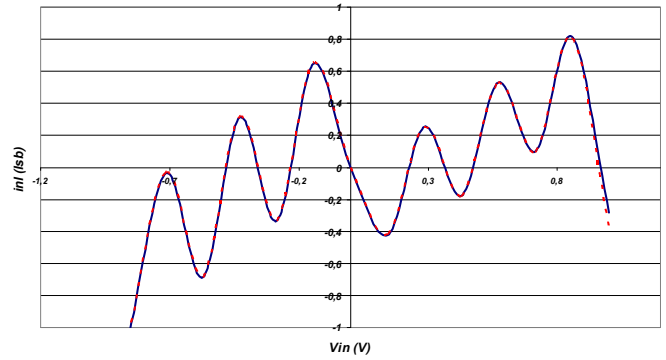


Figure 14: Non linearity of the MDAC 2.5 bit.

This design was submitted in a CMOS 0.35 $\mu$  process from Austria Micro System. The die photograph of the prototype is shown in figure 15.

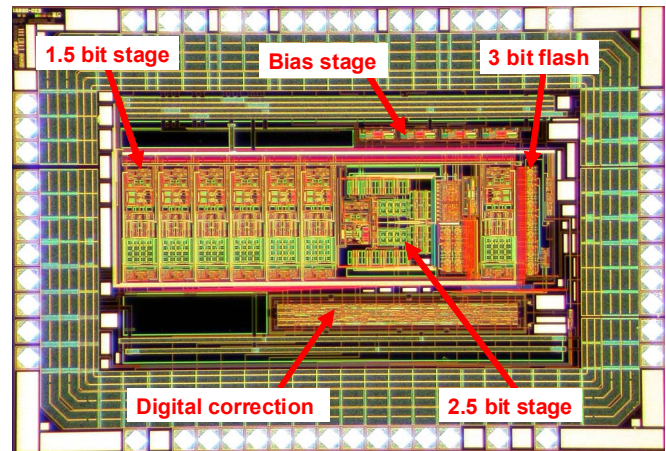


Figure 15: ADC die photograph

### III. TESTING RESULTS

This second prototype has been tested at 25MHz with a power supply of 3.3V. The total power consumption was only 42mW.

In figure 16 and 17 are shown respectively the FFT and the INL for a 1MHz sine wave input signal with 2V peak-to-peak amplitude. The FFT is calculated with 16,384 points.

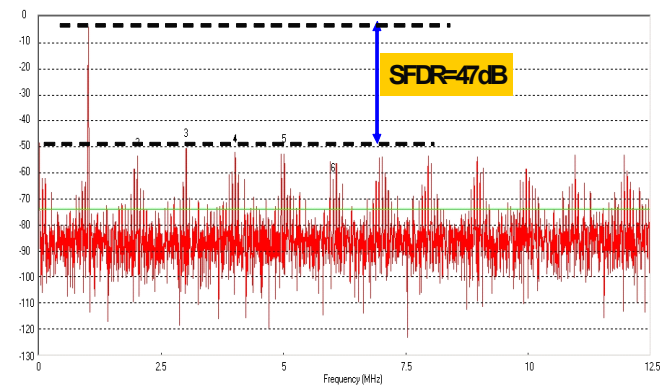


Figure 16: FFT with 16,384 points



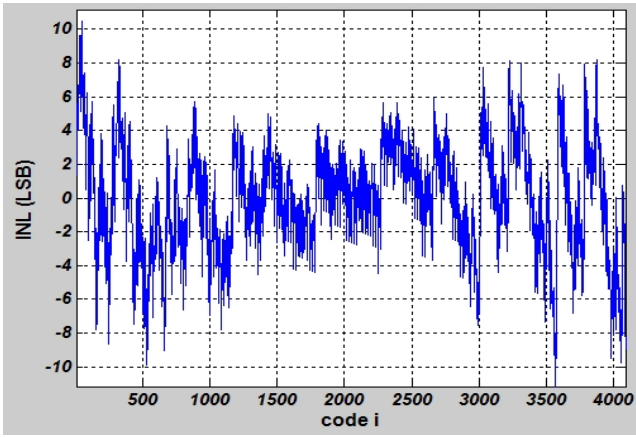


Figure 17: Linearity results (INL)

In this second prototype we have some problem of linearity. Indeed, the SFDR is around 47dB and the INL is up to 8LSB. Two sources for these problems are afterward identified: it was a first version of the layout and the matching of the capacitor need improvement. We discover also a mistake in the value of the threshold voltage in the last full flash ADC; this mistake multiplies by 2 the actual INL.

The output noise distribution is shown in figure 18 for two adjacent output codes. One may notice a RMS noise  $\sigma$  less than 0.6LSB for this ADC.

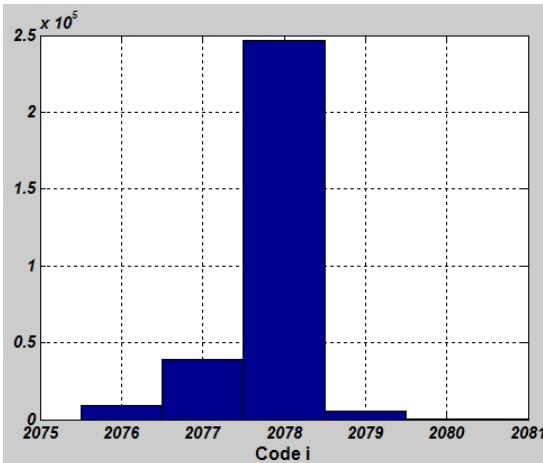
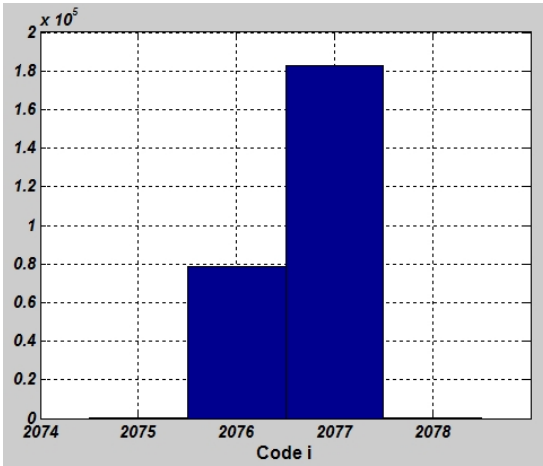


Figure 18: Code edge noise for different dc input

For the next ILC experiment, the beam duty cycle will be very low ( $\sim 0.1\%$ ). It is therefore worthy to switch on the analog part of the circuit only when used, thus making the total power dissipation directly proportional to the beam duty cycle. Therefore, this circuit includes such a fast and efficient “power ON” capability. The settling delay, from the bias pulsing signal up to the converter’s outputs, is given in figure 19. We measured those times by using a sine wave input signal with peak-to-peak amplitude close to the ADC full-scale range (2V).

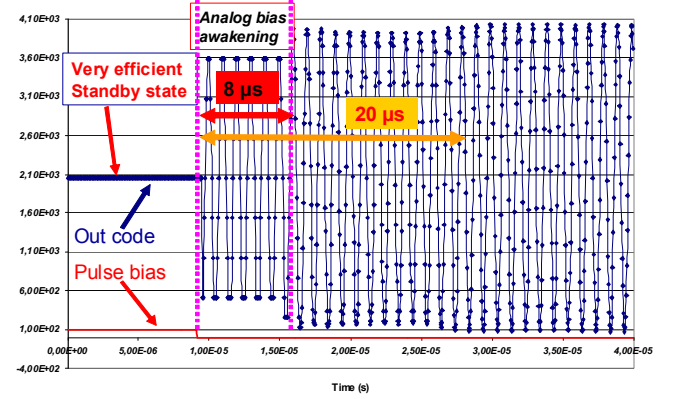


Figure 19: Analog bias fast switching results with sine wave input signal

From the falling edge of a pulsing clock, the bias current is settled after only  $8\mu s$ . In the standby idle mode (pulsing clock at high level), the full analog part of the converter is switched OFF and the analog power dissipation is reduced to a ratio better than 1/1000.

After the analog bias settling, there is an extra recovery time before the full converter can work properly. The input signal for this measurement was a sine wave. One can notice the analog stages settling delay ( $8\mu s$ ); followed by a long recovery time ( $12\mu s$ ) for the full ADC, before then the correct output codes come out.

#### IV. POWER CONSUMPTION

We present in this chapter some results about power consumption of this second version: the 12-bit pipeline A/D converter with a 2.5 bits in the first stage. Those results are presented in table I.

TABLE I  
POWER CONSUMPTION ANALYSIS

	Power ON		Power OFF
	Simulation	Test	Test
Analog	22.6mW	29.1mW	2.11 $\mu$ W
Digital (@25 MHz)	13.1mW		719.4 $\mu$ W
Total	35.7mW	42.2mW	721.5 $\mu$ W

The difference between simulation and test on power consumption of the analog part is mainly due to static comparators. Indeed we need to increase the bias current of comparators to improve some test results as linearity.

For the next ILC experiment, we choose to use only one fast ADC per chip. Each chip is composed of 64-channels and the depth of the analog memory is sixteen. We need to add a multiplexer which made the link between all channels and the ADC. The power consumption of this circuit will be approximately 7mW according to our simulations. The total time conversion is then 41  $\mu$ s by sampling at 25MHz. And the ADC and multiplexer power consumption per chip is about 10 $\mu$ W by using power pulsing concept. This leads into a equivalent power consumption about only 160nW per channel.

## V. CONCLUSION

The design of two prototypes of a 12 bit 25MS/s pipelined ADC has been reported. The first chip consumes very reasonable power dissipation: only 37mW. A 1.5 bit/stage architecture is used for the converter in a differential configuration. An output dynamic range of 80 dB is measured. It has almost  $\pm 1$ LSB of DNL and  $\pm 4$ LSB of INL. This converter is a high speed version for the future International Linear Collider calorimeter detector (CALICE collaboration). The second version has been designed to improve linearity and power dissipation. A 2.5 bits first stage is used in this second chip. A problem of harmonics is coming from parasitic capacitors and matching of capacitors in the first stage. It increases the integral non linearity. This layout problem is fixed for the upcoming prototype. A very efficient fast power pulsing is integrated with this circuit to reduce the total DC power dissipation according to the beam low duty cycle.

## ACKNOWLEDGMENT

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